Charge Transfer Model for SSTL Input Timing
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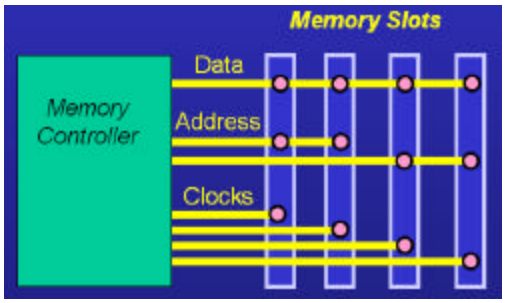
February 2003

Commodity DRAM memories continue to achieve faster data rates and each generation has to struggle with shorter cycle times and tighter timing windows. The Charge Transfer Model was developed as a method for modeling input timing characteristics with finer granularity to help close the tighter timing budgets.

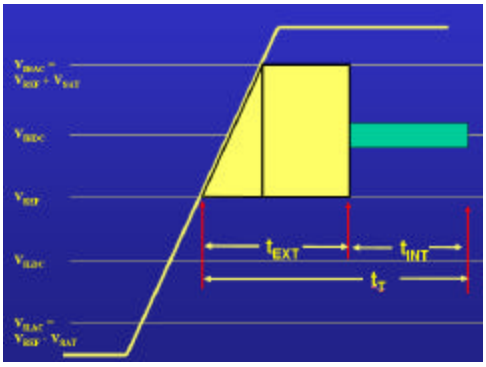
Motherboards like to have memory configurability options yet at the lowest cost. With DDR2 memories, this is typically done with up to four memory slots, any of which can be empty or populated with modules containing 4 to 18 DRAMs directly on a stub-series (SSTL) bus, or up to 36 memories via bus registers.



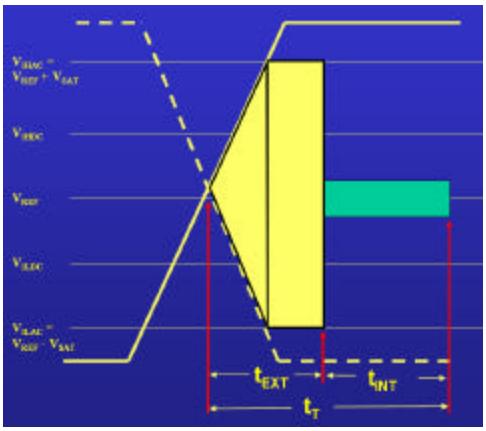
This variability in loading on data, address, command, and clock buses means that input slew rates at the balls of the DRAMs will vary from configuration to configuration, and will not be known until the system boots. Also, it will be nearly impossible to eliminate all non-monotonic transitions on the inputs. The goal of the Model is to define mechanisms for characterizing input transitions and determining the available valid eyes for these buses.

The first assertion of the Model is that SSTL input thresholds are not a function of voltage level crossing but of the area under the input signal curve. This charge accumulates until sufficient energy to kick the input over to the next state is acquired. This charge accumulation is a function of the input signal slew rate, the device package parasitics, and the characteristics of the device input circuit. This accumulation starts, and potentially saturates, at vendor specific levels. However, for the purposes of establishing a JEDEC standard, these levels can be set somewhat arbitrarily to define an envelope for all devices and a common test specification for characterizing compatibility. Also, since DDR2 uses single-ended data, command, and address inputs but differential clocks and strobes, the accumulation characteristics of both input types must be defined.

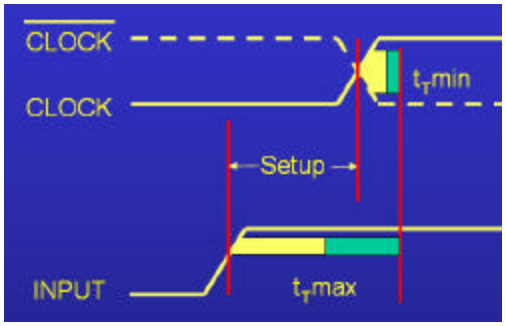
The Model further acknowledges that there are input transition characteristics that are dependent on input slew rate and given a timing value of t_{EXT}, and internal factors such as on-chip routing and internal loading mismatches that are not affected by the incoming waveform and given the timing value t_{INT}. The input transition time t_T is the sum of these.



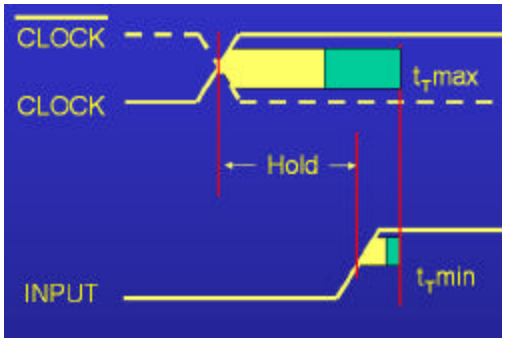
The previous figure shows a model for a single-ended input model with accumulation threshold starting at V_{REF} and saturating at the V_{AC} level. Similarly, the next figure shows a differential input pair accumulating from the crosspoint of the inputs and saturating at the V_{AC} points.



The second phase of the Model is to define setup and hold with respect to these definitions of input transition. Setup is defined as the maximum transition time $t_T$max of an input signal to the minimum transition time $t_T$min of its reference. For DDR2 data, this is the DQ and DM inputs referenced to the DQS strobe pair. For DDR2 addresses and commands, these inputs are referenced to the CK pair.



Similarly, hold time is defined as the maximum transition time $t_T$max of the reference to the minimum transition time $t_T$min of the input signal.



Since single-ended and differential signals derate differently based on the input slew rate, the setup and hold times change in asymmetrical ways as the system loading changes. For this reason, the setup and hold tables for DDR2 are a matrix of inputs and references. Characterizing of the exact values for these tables continues as the industry tests real devices.

SETUP — Strobe (mV/ps avg) / Data (mV/ps)

	0.5	1.0	2.0
0.5	+	+	+
1.0	—	0	+
2.0	—	—	—

SETUP — Clock (mV/ps avg) / Addr (mV/ps)

	0.5	1.0	2.0
0.5	+	+	+
1.0	—	0	+
2.0	—	—	—

HOLD — Strobe (mV/ps avg) / Data (mV/ps)

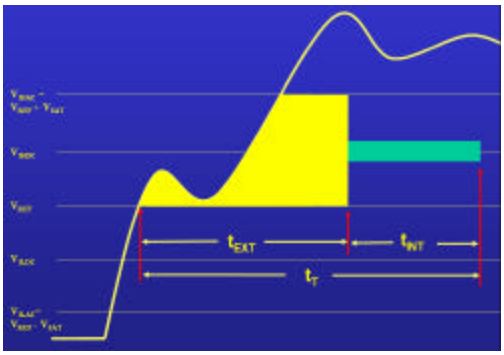
	0.5	1.0	2.0
0.5	+	+	+
1.0	+	0	—
2.0	—	—	—

HOLD — Clock (mV/ps avg) / Addr (mV/ps)

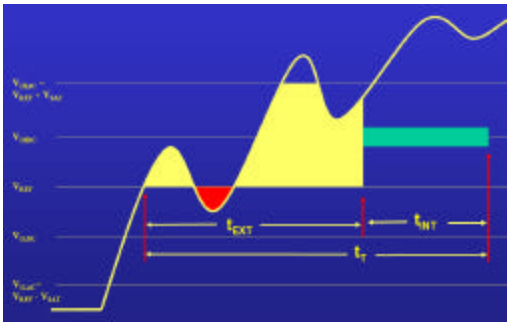
	0.5	1.0	2.0
0.5	+	+	+
1.0	+	0	—
2.0	—	—	—

To fully utilize these tables, a target system such as a PC needs to determine the effects on slew rate of its supported configurations and calculate the available setup and hold time at the DRAM for that configuration. When the system factors such as crosstalk, SSO, ISI, and trace mismatching are added in, an accurate determination of the size of the valid eye for data, address, and command can be calculated.

In this description of the Charge Transfer Model, not much of the actual input characteristic must be known to define an envelope for all suppliers' designs. However, in the future the Model can be expanded to include more knowledge of accumulation and saturation points plus other factors such as power supply and VREF noise to accommodate finer calculation of setup and hold characteristics. One great challenge is to analyze "funky" signals with shelves or slope reversals due to line termination imperfections.



In the simplest case, the slope reversals simply delay the charge accumulation until sufficient charge is built up to force the input state transition. In more complicated cases, reversals that drop below the accumulation level can subtract from the charge accumulation, further delaying the transition, but in a way that can be determined with some accuracy.



The Charge Transfer Model is a tool for system designers to use to seek out available performance headroom in high frequency systems. By analyzing the input slew rates in a given configuration and knowing the impact on setup and hold times, the Model yields a way to determine the maximum frequency at which the system configuration can operate.

In the future, the Charge Transfer Model promises to help support wider configuration options and system topologies with the same confidence that we have in today's designs.