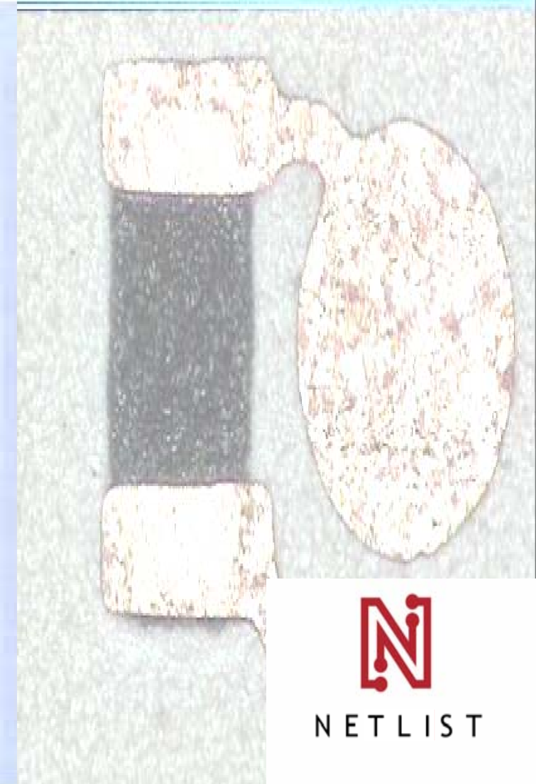
Embedded Passives in Memory Modules

January 25, 2005

Bill Gervasi
Senior Technologist
Netlist, Incorporated
bgervasi@netlistinc.com



Netlist

- Manufacturer of very high density memory modules
- Based on JEDEC industry standards
- Propose new industry standards
  - Chairman of
    - DRAM packaging committee
    - Small Modules committee
    - 4 Rank Module Task Group
- Currently in production with embedded resistors
- Also use embedded capacitors for labs, future production use planned

NETLIST

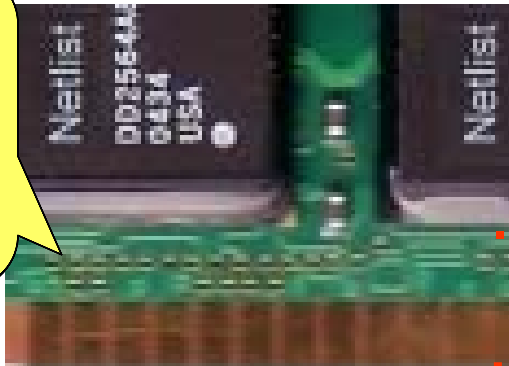
Performance Requirements

- Today's DRAM interfaces
  - Running at 400, 533, 667, 800MT/s per pin, 72 bits wide
  - Command rate ½ of DRAM interface rate
- Next generation (2007)
  - DRAM interfaces to 1600MT/s per pin
  - Controller-hub interfaces at 4.8GHz → 9.6GHz

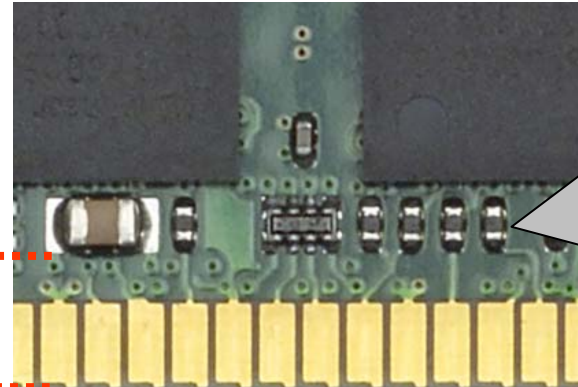
NETLIST

Why Embedded Passives?

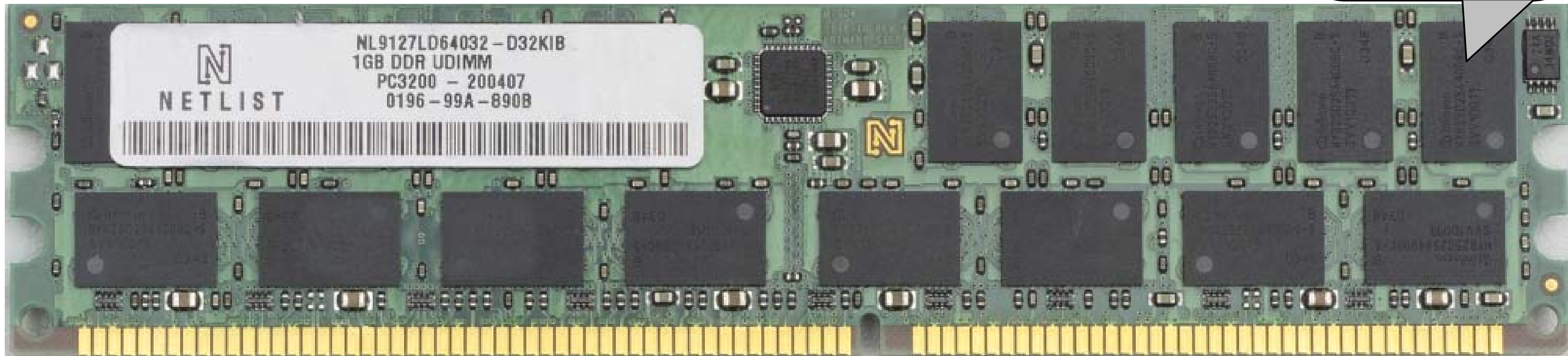
Using embedded resistors



4 mm keepout



Using SMT resistors



Why Embedded Passives?

Using embedded resistors

Saves space for what my customers pay for: DRAMs

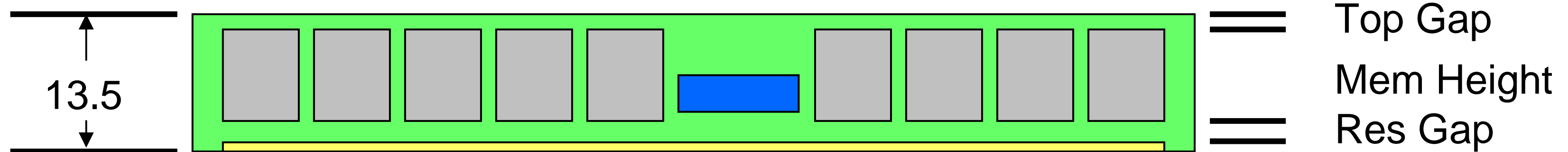
Improves signal integrity due to ability to place components where needed

Reduces manufacturing cost – break even at 65 replaced SMT placements

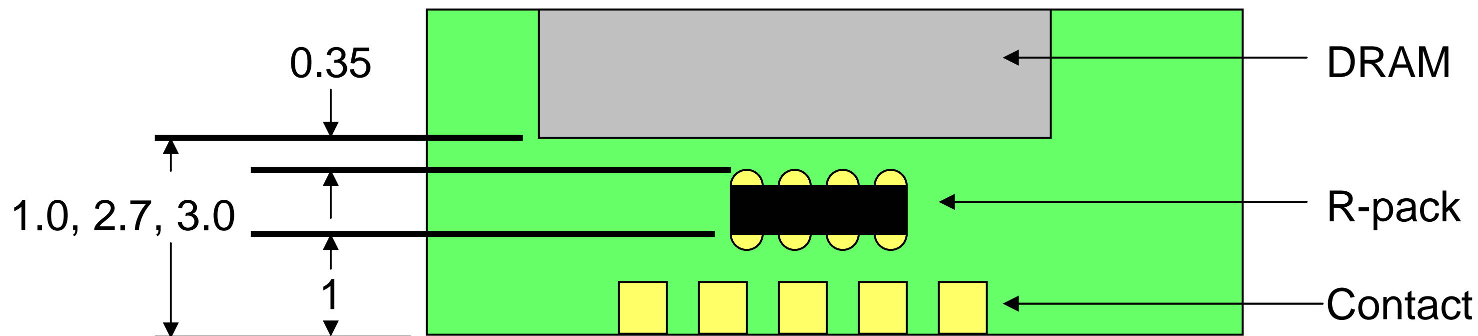
Increases module reliability – eliminates #1 failure mechanism in production

Using SMT resistors

Very Low Profile Memory Module



	Top Gap	Res Gap	Mem Height
EP	0.3	0	12.2
0201 res	0.3	1.7	10.5
0402 res	0.3	2	10.2



DDR2 512Mb BGA Comparison

	Monolithic	Stack 1	Stack 2	Stack 3
AAA	12x19	12x19	16x20	12x19.2
BBB	11x13	11x13	15x14	12x13.2
CCC	11x11.5	11x11.5	15x12.5	12x11.7
DDD	10x10.5	10x10.5	14x11.5	12x10.7
EEE	10x11.2	10x11.2	14x12.2	12x11.4
FFF	12x14	12x14	16x15	12x14.2
GGG	11.3x13.8	11.3x13.8	15.3x14.8	12x14.0

All DRAM sizes are different

DDR2 VLP FrameDIMM

Monolithic

EP	0201	0402
CCC	DDD	DDD
DDD	EEE	EEE
EEE		

Stack 1

EP	0201	0402
CCC	DDD	DDD
DDD	EEE	EEE
EEE		

Stack 2

EP	0201	0402

Stack 3

EP	0201	0402
CCC		
DDD		
EEE		

NETLIST

Embedded Capacitor Geometries

Decoupling		CFP Area	CFP sq	CFP c-dia
		mm2	mm	mm
10	uF	645390.30	803.36	906.50
4.7	uF	303333.44	550.76	621.46
2.2	uF	141985.87	376.81	425.18
1	uF	64539.03	254.05	286.66
470	nF	30333.34	174.16	196.52
220	nF	14198.59	119.16	134.46
100	nF	6453.90	80.34	90.65
47	nF	3033.33	55.08	62.15
22	nF	1419.86	37.68	42.52
10	nF	645.39	25.40	28.67
4.7	nF	303.33	17.42	19.65
2.2	nF	141.99	11.92	13.45
DRAM Sim:		CFP Area	CFP sq	CFP c-dia
		mm2	mm	mm
15.500	pF	1.00	1.00	1.13
5.000	pF	0.32	0.57	0.64
4.500	pF	0.29	0.54	0.61
4.000	pF	0.26	0.51	0.57
3.500	pF	0.23	0.48	0.54
3.250	pF	0.21	0.46	0.52
3.000	pF	0.19	0.44	0.50
2.500	pF	0.16	0.40	0.45
2.000	pF	0.13	0.36	0.41
1.500	pF	0.10	0.31	0.35
1.000	pF	0.06	0.25	0.29
0.790	pF	0.05	0.23	0.25

Future needs

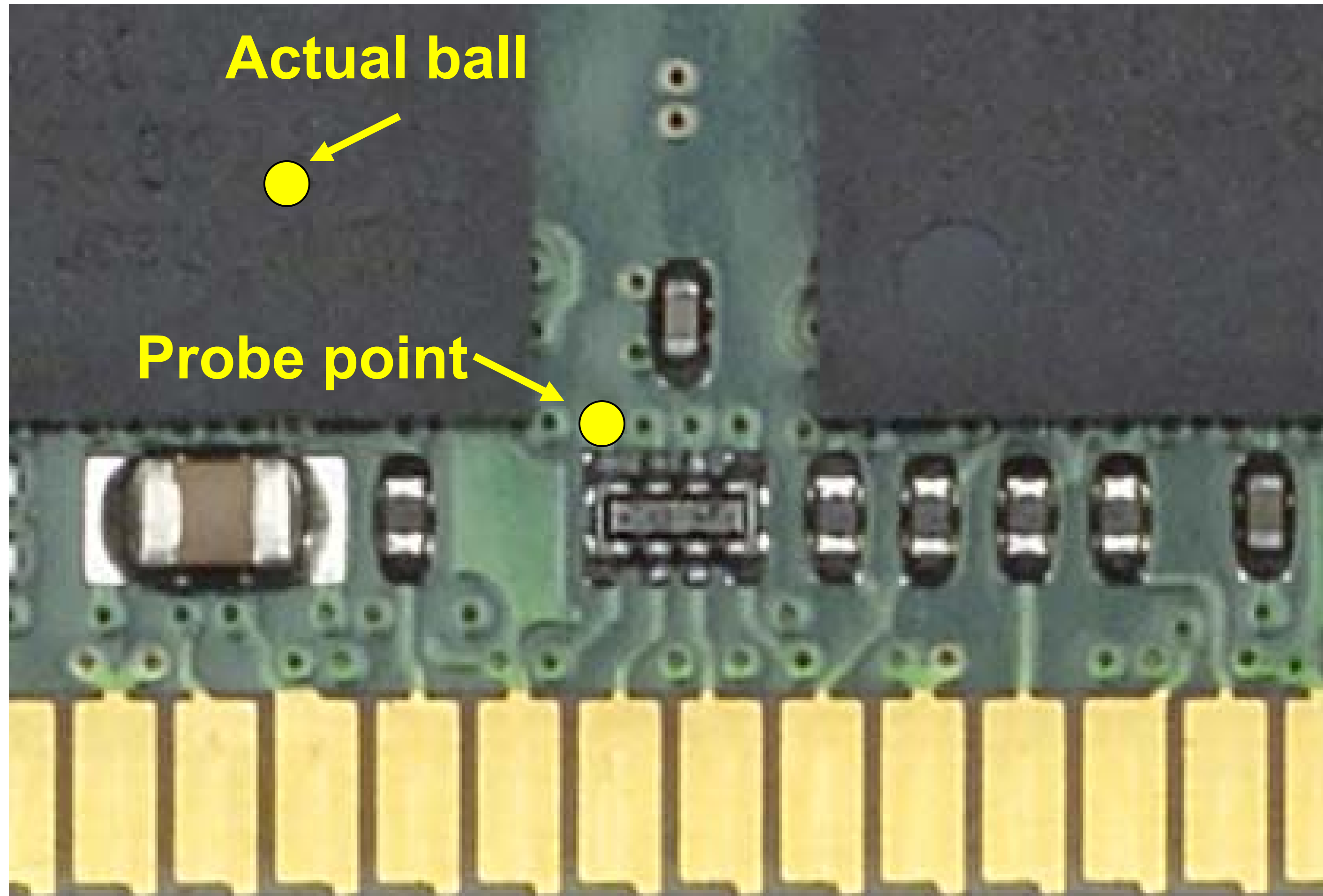
-----

3 nF/mm^2 evaluation in 1Q05

Realistic now

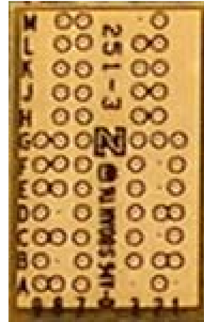
- Need small micron to sub-micron dielectrics
- Using rolled on CFP (Motorola process)

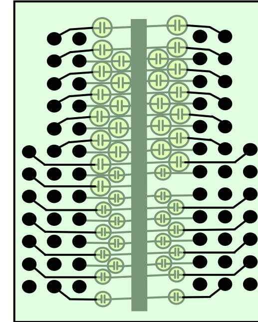
Probing BGA-based designs



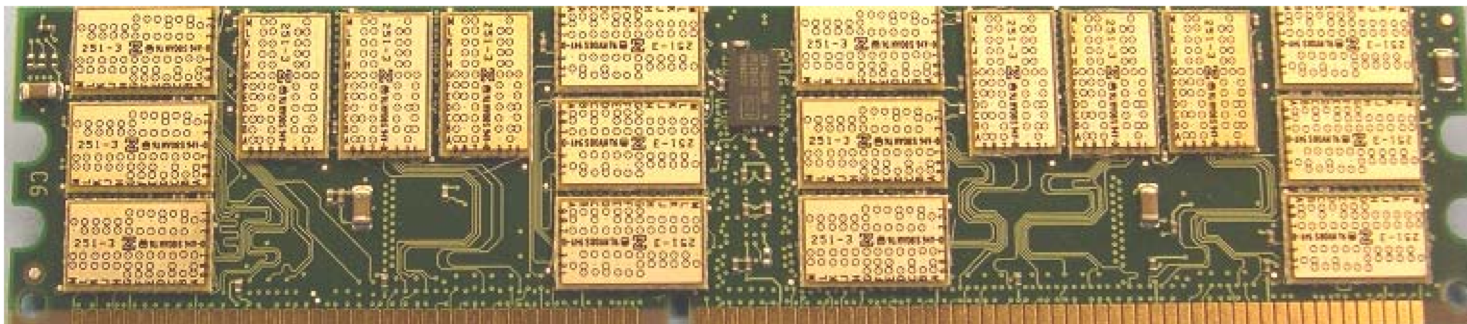
NETLIST

DRAM Load Simulator (DLS)





- BGA substrate with DRAM footprint below
- Top surface has probe points for all signals
- Per-signal internal load matching pF-class capacitors

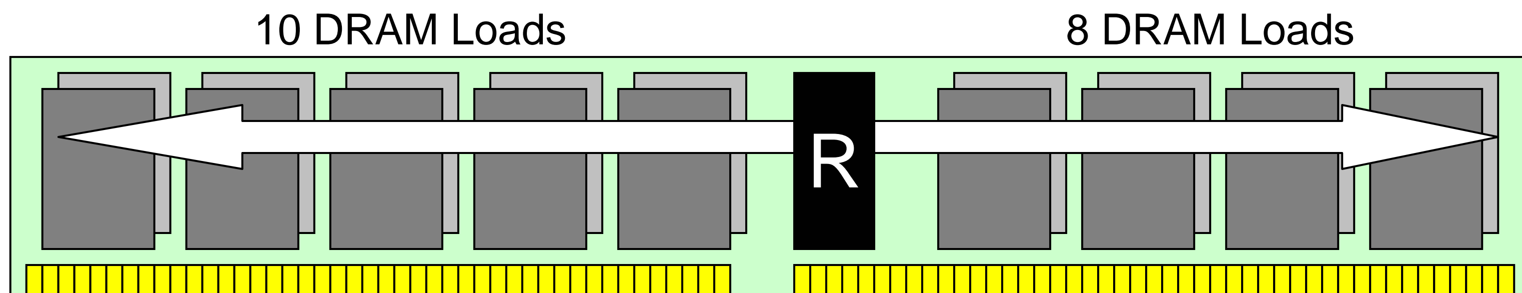


NETLIST

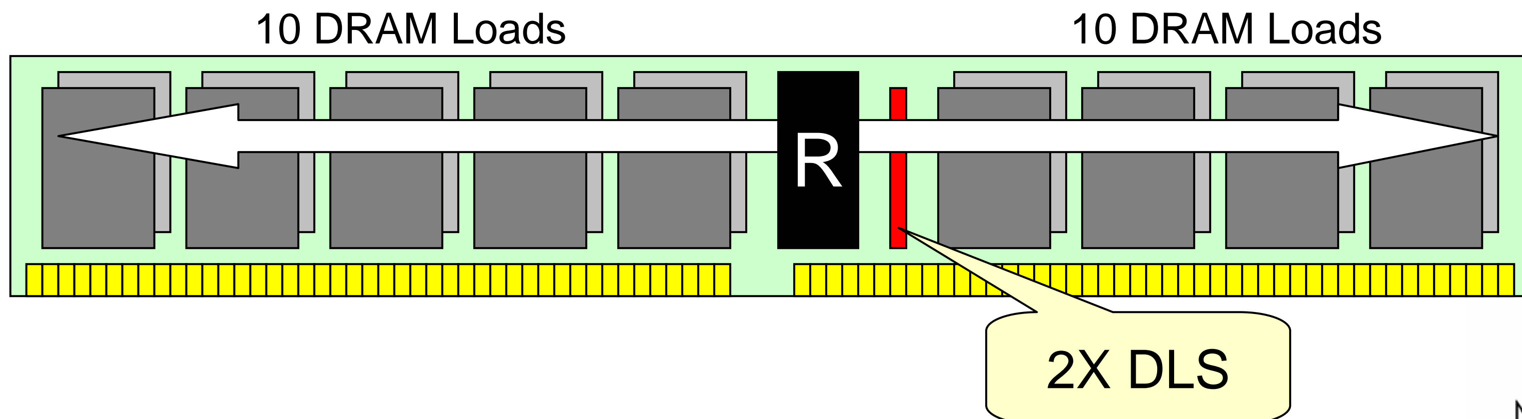
Load Matching 1:2 Register Outputs

- With 18 DRAM sites, hard to balance as 9+9 loads

∴ Tight layouts often have 10+8 loads



- Embedded 2X strength DLS can balance both sides



Reliability of Embedded Resistors

- Screened polymer thick film, Motorola process
- One value of ink (50Ω), one screening
- 110 resistors @ 22Ω nominal
- 20 resistors @ 60Ω nominal

NETLIST

Summary of Life Tests

Bare Boards	• Exhibit A: Testing the same resistors through 2 reflows, a bake, then 10 more reflows • Exhibit B: Heat soak, thermal cycle, humidity • Exhibit C: Testing the same resistors over repeated thermal cycling • Exhibit D: 3-axis vibration
Assembled Boards	• Exhibit E: Biased humidity testing
Simulation	• Exhibit F: Impact on system timing at margin • Exhibit G: Tolerance push to failure

NETLIST

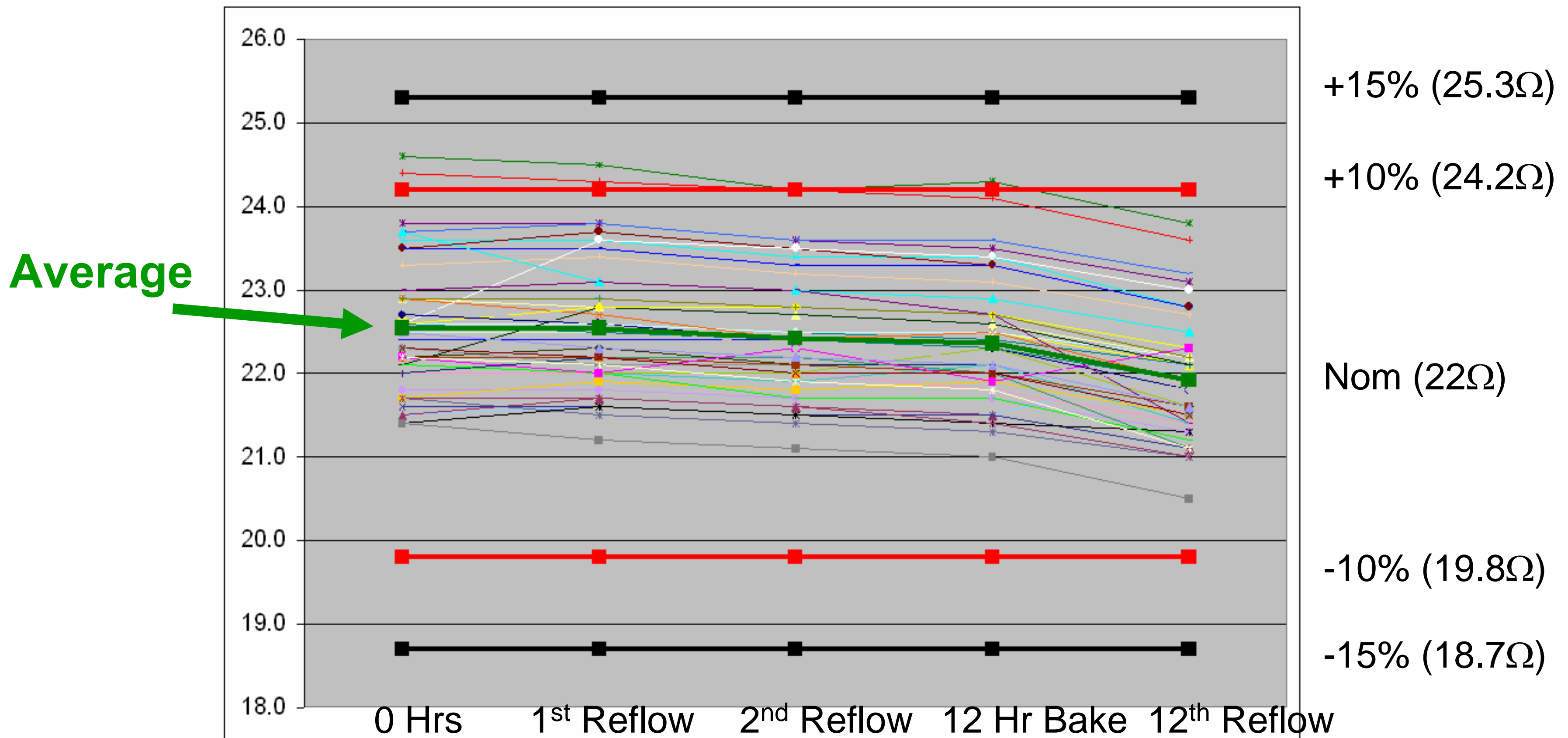
Buried Resistor Tolerance Over Thermal Shock

Purpose: Six resistors per board tested at multiple cycle points during heat testing, all 110 resistors tested before and after thermal stress

1. Measure resistance
2. Reflow @ 220 °C
3. Measure
4. Reflow @ 220 °C
5. Measure
6. 55 °C bake for 12 hours
7. Measure
8. Reflow 10 times @ 220 °C
9. Measure

NETLIST

All Boards, All Resistors



22.5	22.5	22.4	22.4	21.9

Average:

Δ = -0.1 Ω, 2 reflows

Δ = -0.5 Ω, 12 reflows

NETLIST

Buried Resistor Tolerance Under Thermal Stress

Purpose: Application of heat soak, thermal cycle, and humidity

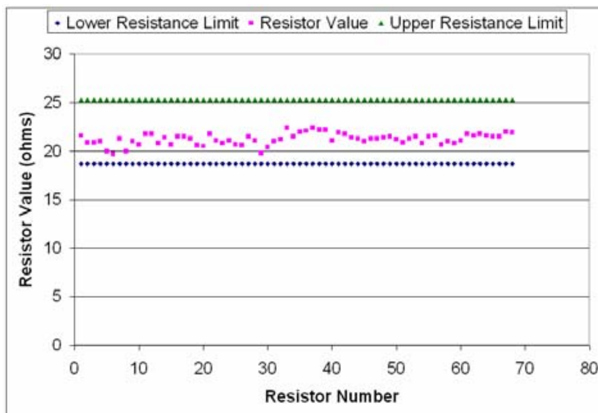
Heat soak: 150°C

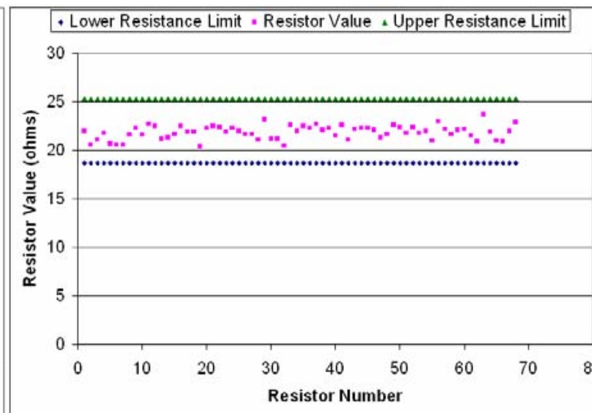
Thermal cycle: -10°C to +115°C @ 3°C/minute
Humidity: RH 85% at 85°C, module powered to 2.5V

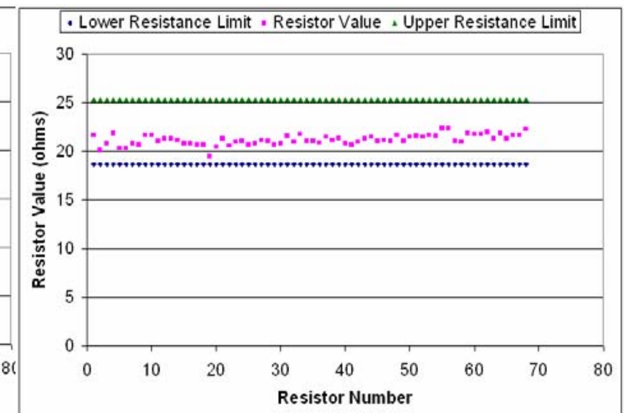
NETLIST

Embedded Resistors: Thermal Shock

Conditions:	Conditions:	Conditions:
500 hours of heat soaking	500 hours of thermal cycling	500 hours of humidity stress







NETLIST

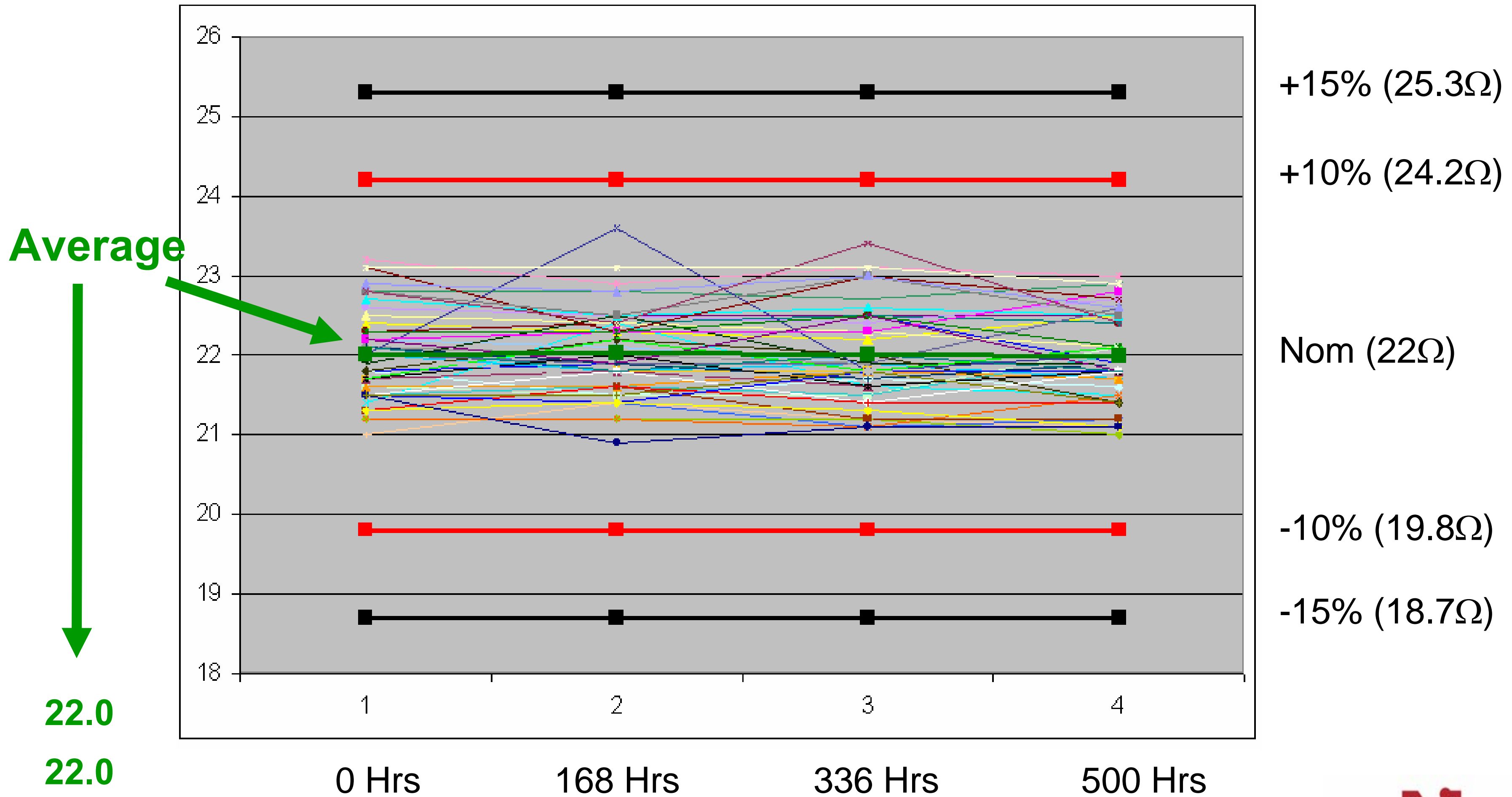
Buried Resistor Tolerance and Drift & Analyze Probing Accuracy

Purpose: Analyze drift for same resistors over 500 thermal cycles on the same board. Analyze tester tolerance.

Method: Thermal cycle: -10°C to +115°C @ 3°C/minute

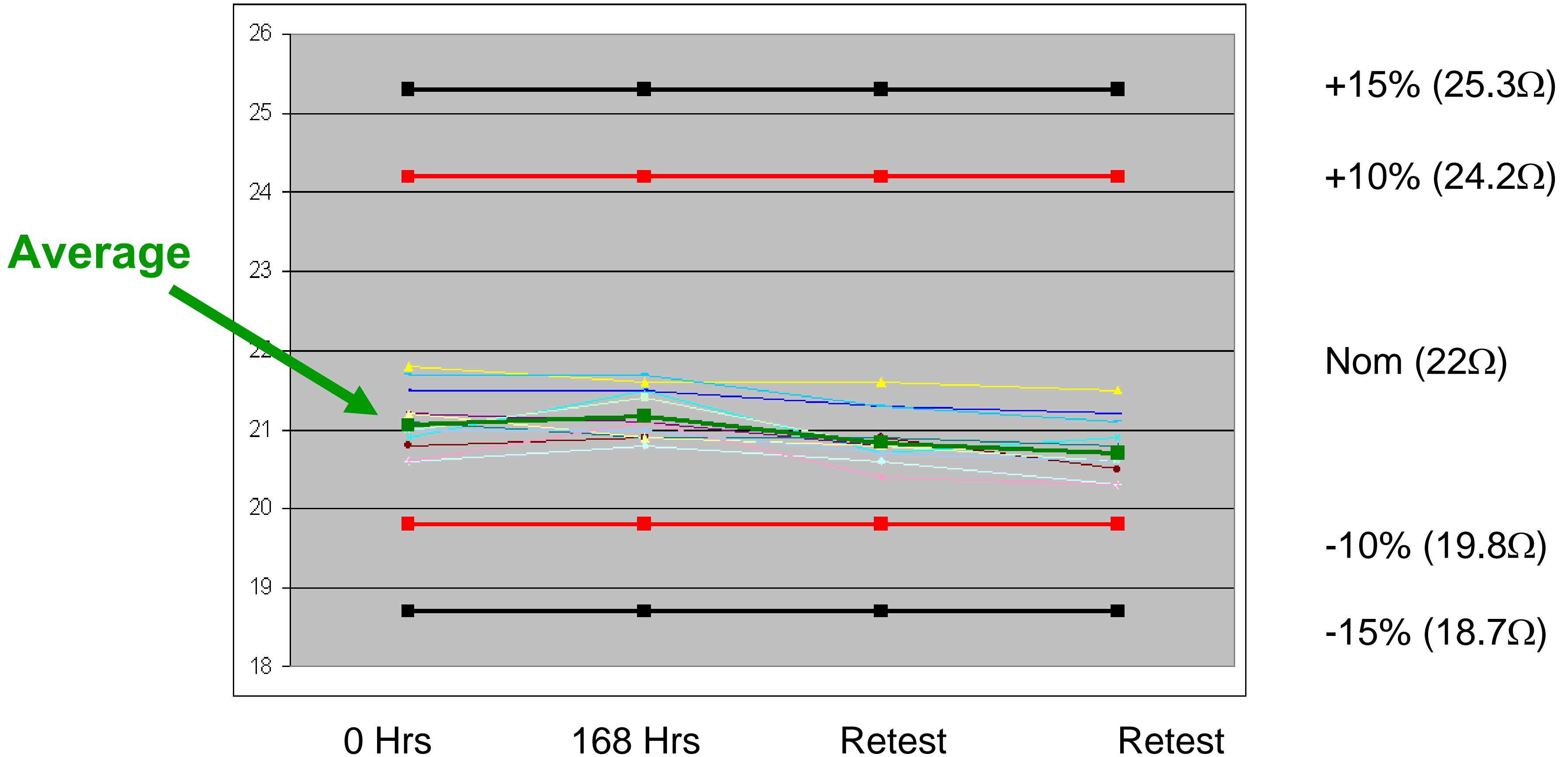
NETLIST

Resistor Values Over Cycling



NETLIST

Resistor Sampling Error



												Average
21.8	20.9	21.2	20.8	21.1	21.5	21.7	20.6	21.0	21.2	21.0	20.6	21.1
21.6	21.5	21.1	20.9	20.9	21.5	21.7	20.8	21.4	20.9	21.0	21.1	21.2
21.6	20.7	20.8	20.9	20.9	21.3	21.3	20.6	20.8	20.8	20.7	20.4	20.8
21.5	20.9	20.7	20.5	20.8	21.2	21.1	20.3	20.6	20.7	20.6	20.3	20.7

NETLIST

Buried Resistor Vibration Screening

Purpose: Determine impact of mechanical stress on buried resistors due to vibration shock in 3 axes

Method: Tri-axial random vibration system from 0 to $20G_{RMS}$ in 5G increments, 30 minutes at each stage

NETLIST

Vibration Testing

- 30 modules selected from 5 panels
- 118 resistors checked per module
- 3540 resistance measurements taken for errors caused by vibration at each stage
- 17700 total checks

- Zero Failures Detected

NETLIST

Buried Resistor Biased Humidity Test of Assembled Modules

Purpose: Verify module functionality after temperature and humidity stress with applied voltage bias; look for migration of resist material

Method: 85ºC/85% RH

500 Hours

NETLIST

Design Rules for Buried Resistors

PTF BURIED RESISTORS (Motorola Process)

3 MIN TRACE
SILVER LAND AREA
PTF RESISTOR MATERIAL
L
W
32
24
20
10 MIN
10 MIN
15 MIN
10 MIN (from resistor to any copper)
(3 mil from antipad to trace)
ANTIPAD
FEEDTHRU

	Width (W)	Length (L)	OHMS	Tolerance
MILS	11	25	22	+/-15%

Note: All dimensions are in mils

Summary for Exhibit E Testing

- No failures detected
- No visual evidence of erosion
- No visual evidence of filament growth

- Conclusion: No evidence of problems with voltage biased humidity testing

NETLIST

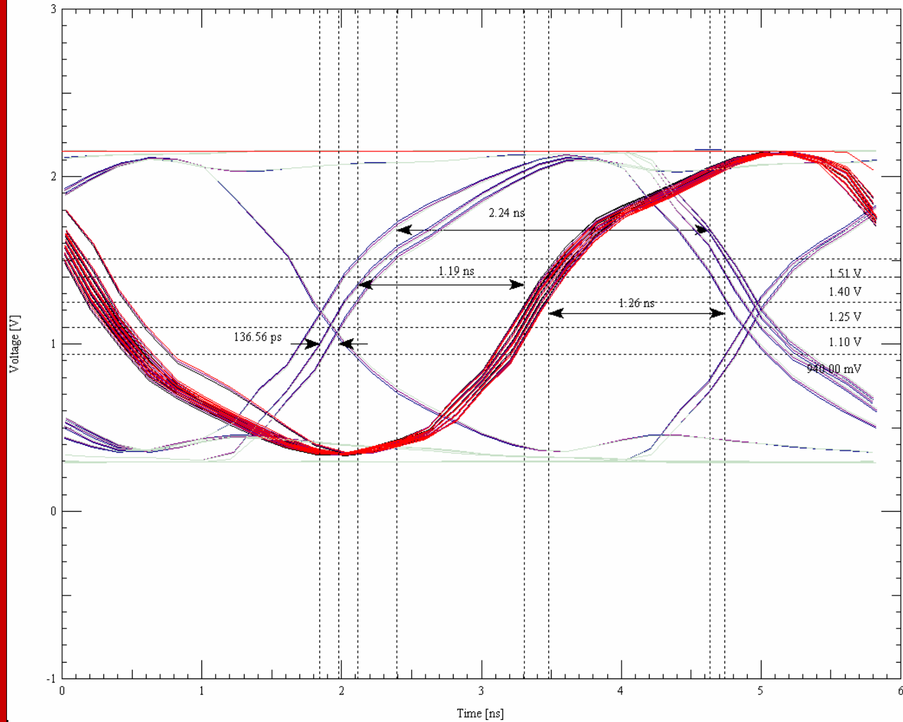
Buried Resistor Tolerance
Timing Impact, Simulation

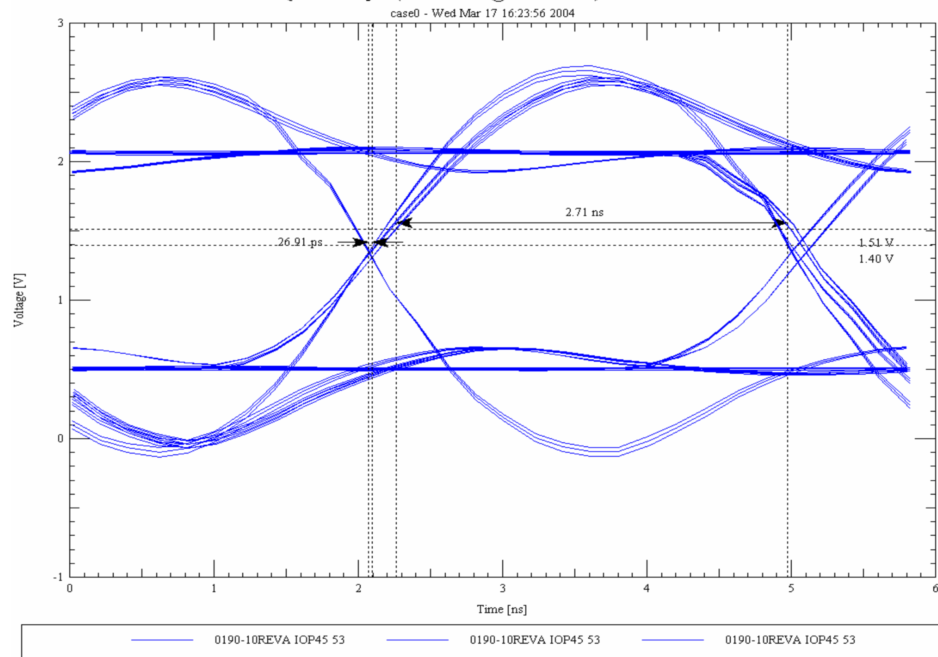
Purpose: Analyze impact of 20% resistor tolerance

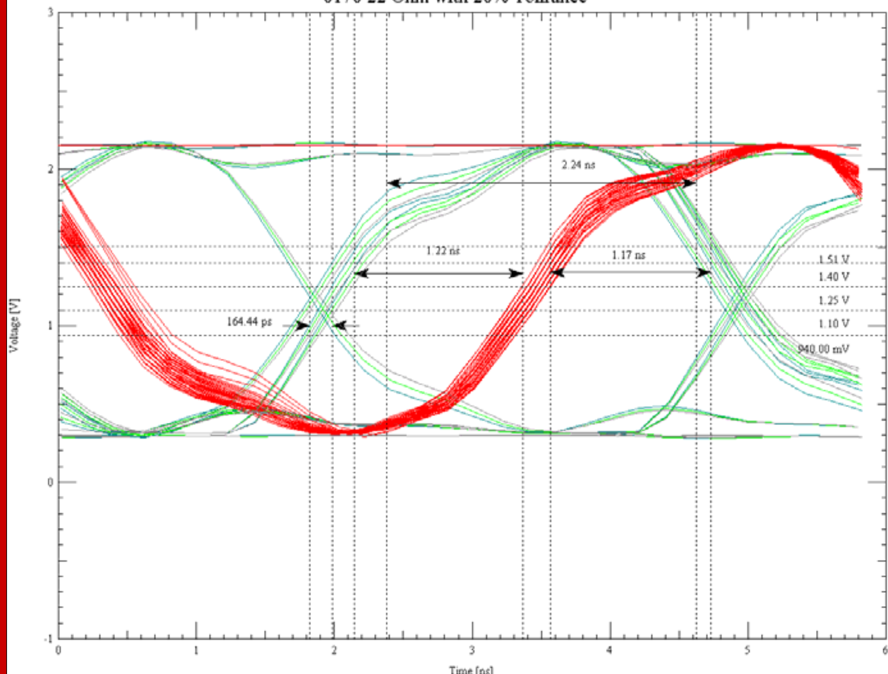
Method: Compare 22 Ω ±20% to JEDEC standard 22 Ω ±5%

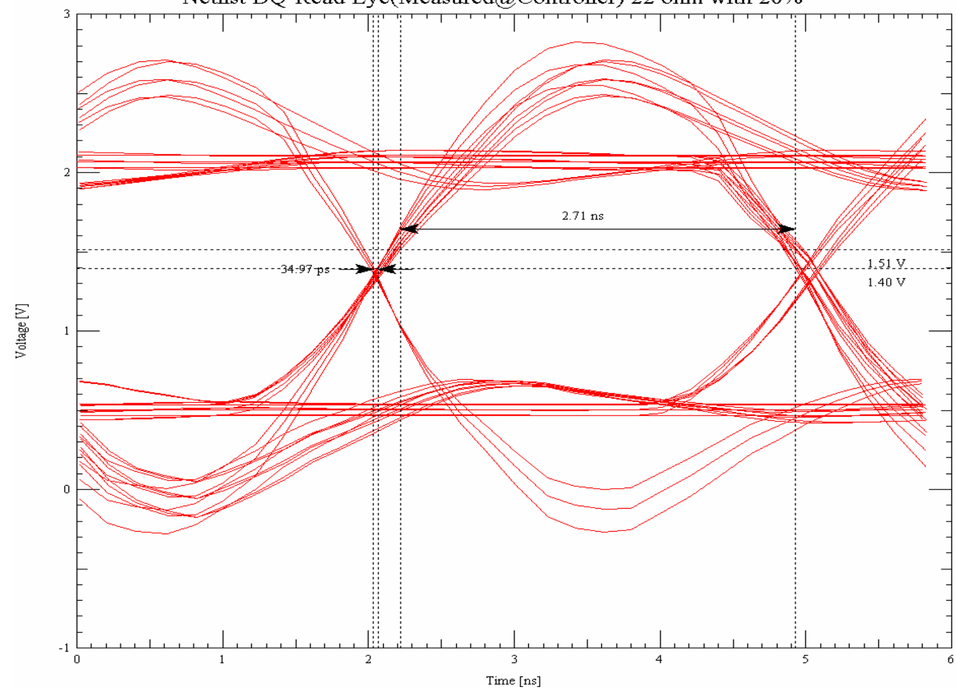
Series damping on data and strobe

NETLIST


Jedec 22 Ohm with 5% Tolerance
Voltage [V]
Time [ns]
2.24 ns
1.19 ns
1.26 ns
136.56 ps
1.51 V
1.40 V
1.25 V
1.10 V
940.00 mV


Jedec DQ-Read Eye (Measured@controller) 22 ohm with 5%
case0 - Wed Mar 17 16:23:56 2004
Voltage [V]
Time [ns]
2.71 ns
26.91 ps
1.51 V
1.40 V
0190-10REVA IOP45 53
0190-10REVA IOP45 53
0190-10REVA IOP45 53


0170 22 Ohm with 20% Tolirance
Voltage [V]
Time [ns]
2.24 ns
1.22 ns
1.17 ns
164.44 ps
1.51 V
1.40 V
1.25 V
1.10 V
940.00 mV


Netlist DQ-Read Eye(Measured@Controller) 22 ohm with 20%
Voltage [V]
Time [ns]
2.71 ns
34.97 ps
1.51 V
1.40 V

Timing Comparison

JEDEC:

WRITES:

tDV = 2.24 ns

READS:

tDV = 2.71 ns

Netlist:

WRITES:

tDV = 2.24 ns

READS:

tDV = 2.71 ns

Conclusion: Identical timing within <10ps in critical voltage region

NETLIST

Buried Resistor Tolerance Pushed to Failure, Simulation

Purpose: Determine how far embedded resistor tolerance can drift before system failure occurs

Method: Simulation of DDR2 system environment to slow/slow and fast/fast corners with resistor tolerance beyond design guardband spec of ±20%

NETLIST

1.10 V _ Vih (AC)
975.00 mV_Vih(DC)
834.29 mV (Vix)
725.00 mV _Vil(DC)
600.00 mV_Vil(AC)

/DQS
DQ
DQS

1.09 ns (11 tDS)
1.07 ns (15.4 tDS)
1.04 ns (19.8 tDS)
1.03 ns (22 tDS)
1.02 ns (24.2 tDS)
998.78 ps (28.6 tDS)
976.41 ps (33 tDS)

1.12 ns (11 tDH)
1.10 ns (15.4 tDH)
1.08 ns(19.8 tDH)
1.07 ns (22 tDH)
1.06 ns (24.2 tDH)
1.04 ns (28.6 tDH)
1.03 ns (33 tDH)

Voltage [V]
Time [ns]

/DQS
DQ
1.20 V _ Vih (AC)
921.68 mV (Vix)
700.00 mV_Vil(AC)
DQS

468.11 ps (11_DQS_F)
470.64 ps (15.4_DQS_F)
471.78 ps (19.8_DQS_F)
472.03 ps (22_DQS_F)
472.77 ps (24.2_DQS_F))
476.02 ps (28.6_DQS_F)
479.45 ps (33_DQS_F)

456.00 ps (11_DQS_R))
460.63 ps (15.4_DQS_R)
461.71 ps(19.8_DQS_R)
461.83 ps (22_DQS_R)
463.22 ps (24.2_DQS_R)
467.52 ps (28.6_DQS_R)
474.43 ps (33_DQS_R)

Voltage [V]
Time [ns]

Summary for Push to Failure Simulation

- Writes:

	-50%		-30%		-10%		Nom		+10%		+30%		+50%	
	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓
Δt normalized (ps)	+60	+50	+40	+50	-10	+10	0	0	-10	-10	-40	-30	-70	-40

- Reads:

Δt normalized (ps)	-5	-4	-1	-2	0	-2	0	0	+2	0	+6	+4	+13	+7

NETLIST

Summary

- Exhibit A: Reflow (Bare board)
  - 0.5% drift with normal stress, 2.3% extreme stress
- Exhibit B: Soak, cycle, humidity (Bare board)
  - Tolerance acceptable over stresses
- Exhibit C: Value drift (Bare board)
  - No detectable drift over stress, probing accuracy 0.5 Ω
- Exhibit D: Vibration (Bare board)
  - No failures detected
- Exhibit E: Biased humidity (Assembled board)
  - No failures detected
- Exhibit F: System timing (Simulation)
  - Meets JEDEC standard timing
- Exhibit G: Push to failure (Simulation)
  - System timing should be okay at ±30% or better

NETLIST

Current Status

- Production for over a year
- Many tens of thousands of boards shipped
- Zero failures in manufacturing*
- Zero failures in customer base*

* *Attributable to embedded passives*

Next Steps

- Better simulation models for buried components
- Improve resistor tolerance <10% without trimming
- Replace decoupling caps (90-ish @ 100nF)
  - Two per DRAM: VDD & VREF
  - 10x10mm footprint
  - Using one layer of capacitors for both sides of the board

NETLIST