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Time to Rethink DDR4

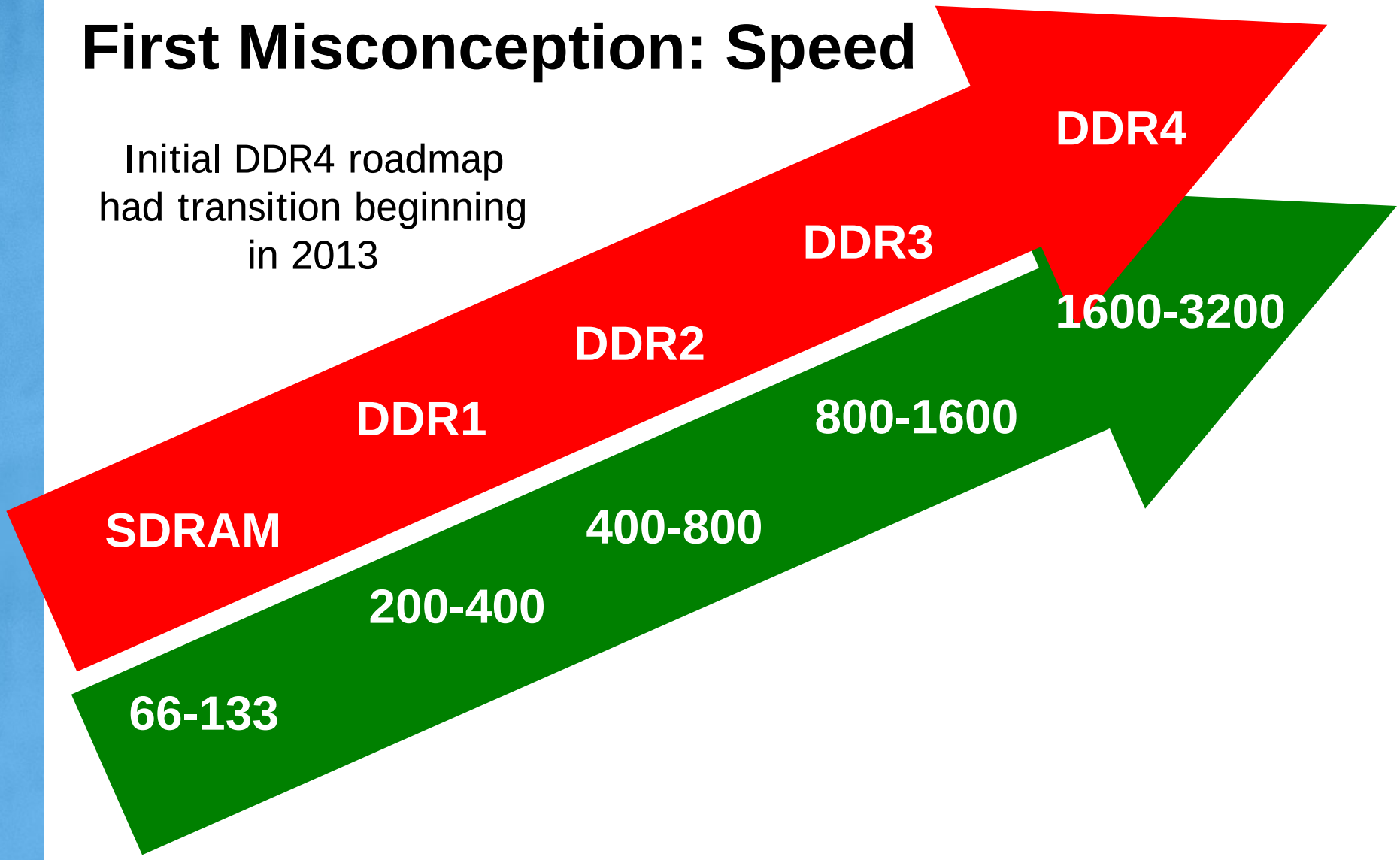
Bill Gervasi

July 2010

DISCOBOLUS DESIGNS

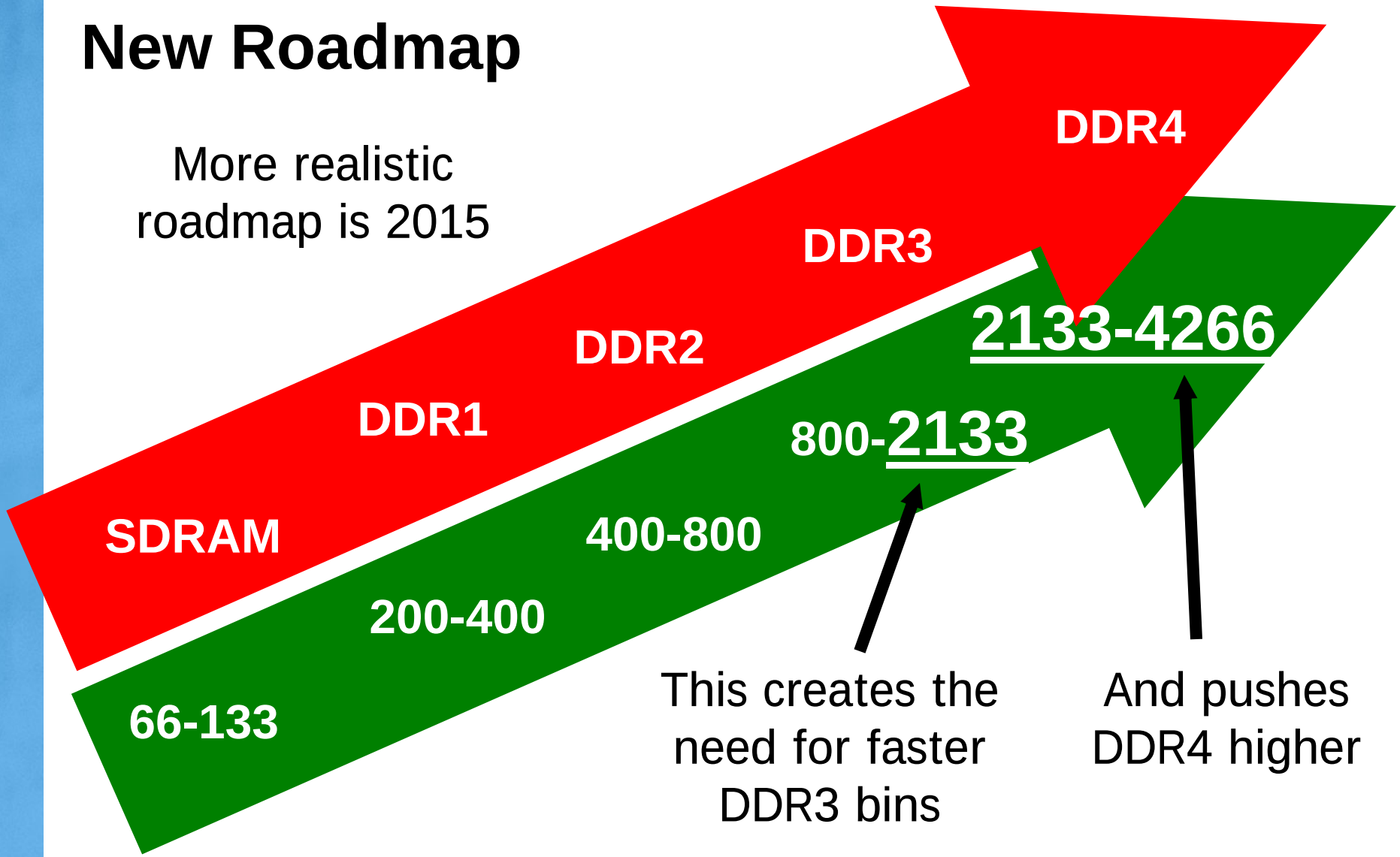
First Misconception: Speed

Initial DDR4 roadmap had transition beginning in 2013

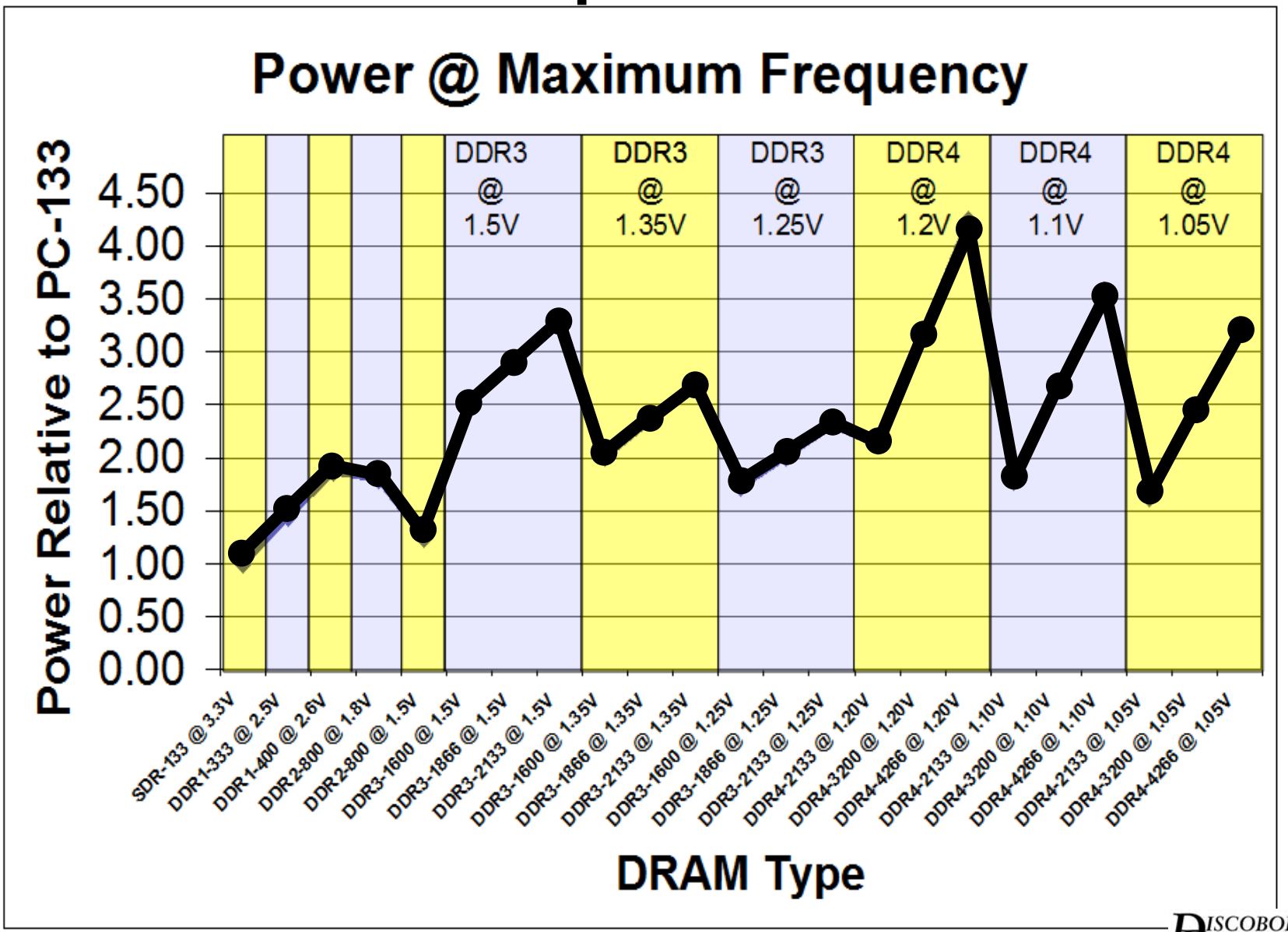


New Roadmap

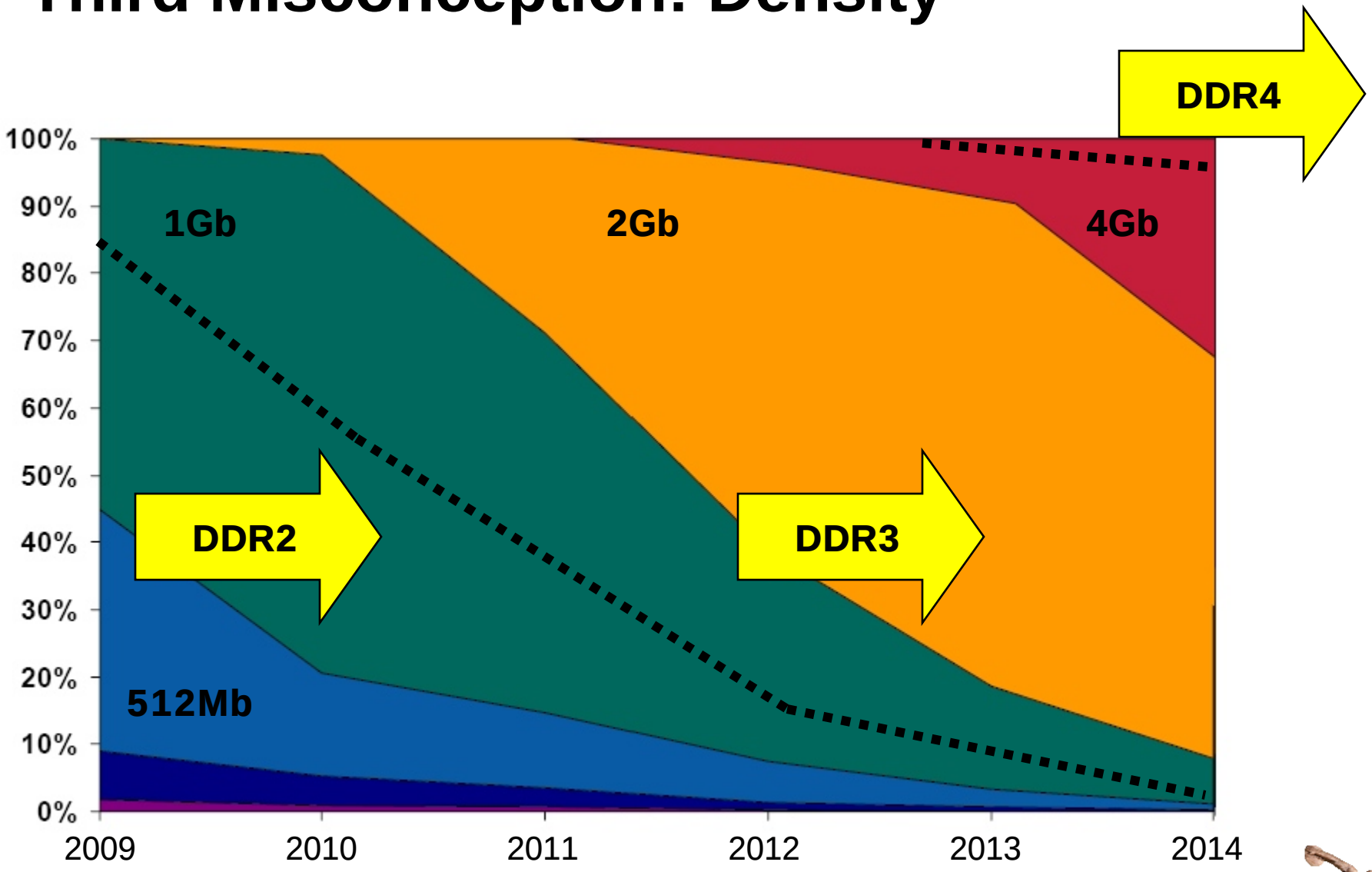
More realistic roadmap is 2015



Second Misconception: Power



Third Misconception: Density



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Fragmentation Creates Delays

- Reality is that power is out of control
- DDR3 1.5 → 1.35 → 1.25V

This is diverting engineering resources

- Low Voltage DDR3 will delay DDR4
- LV DDR3 will delay 4Gb and 8Gb

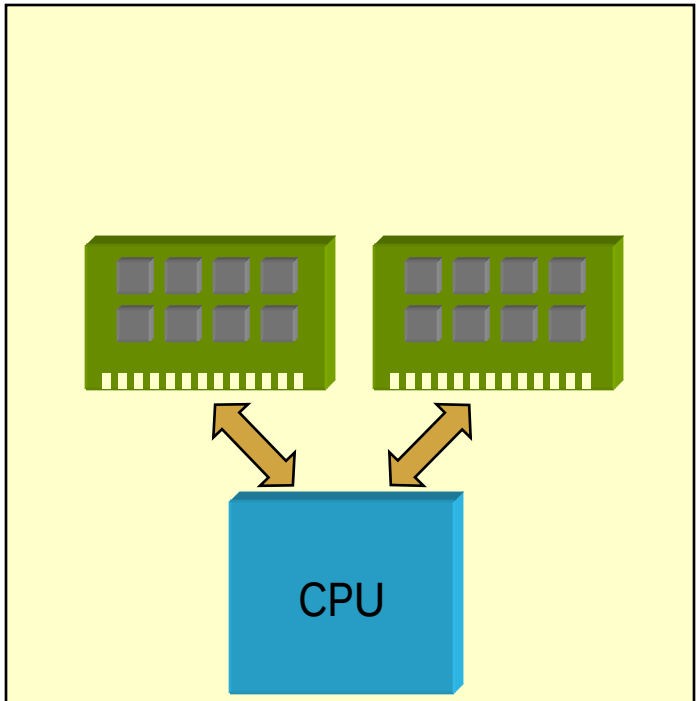
Impacts on Modules

- Multi-drop bus must die
- Point to point connections required for high frequency operation
- Single load DRAM stacks change the foundation

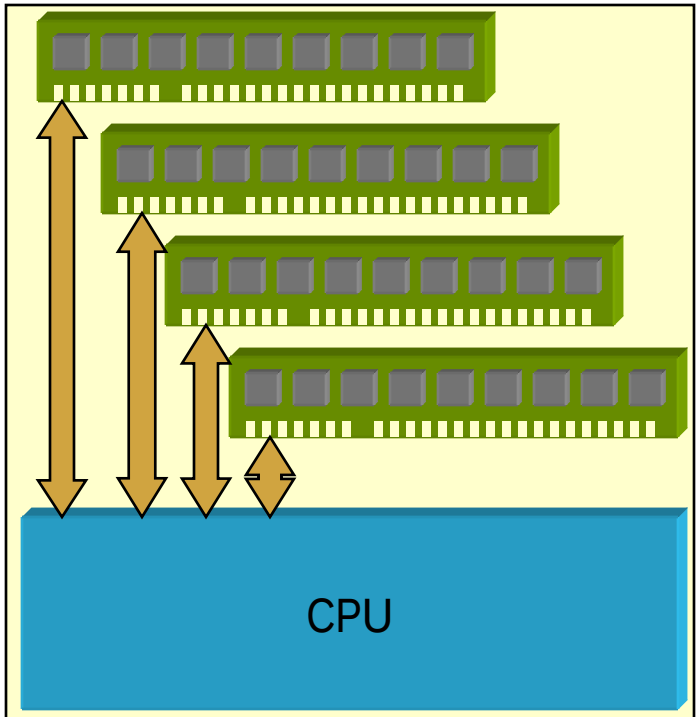
  LR-DIMM will be another point solution unless single load stacks fail

- RDIMM may live on to alleviate address bus challenges

Modules in DDR4 Generation

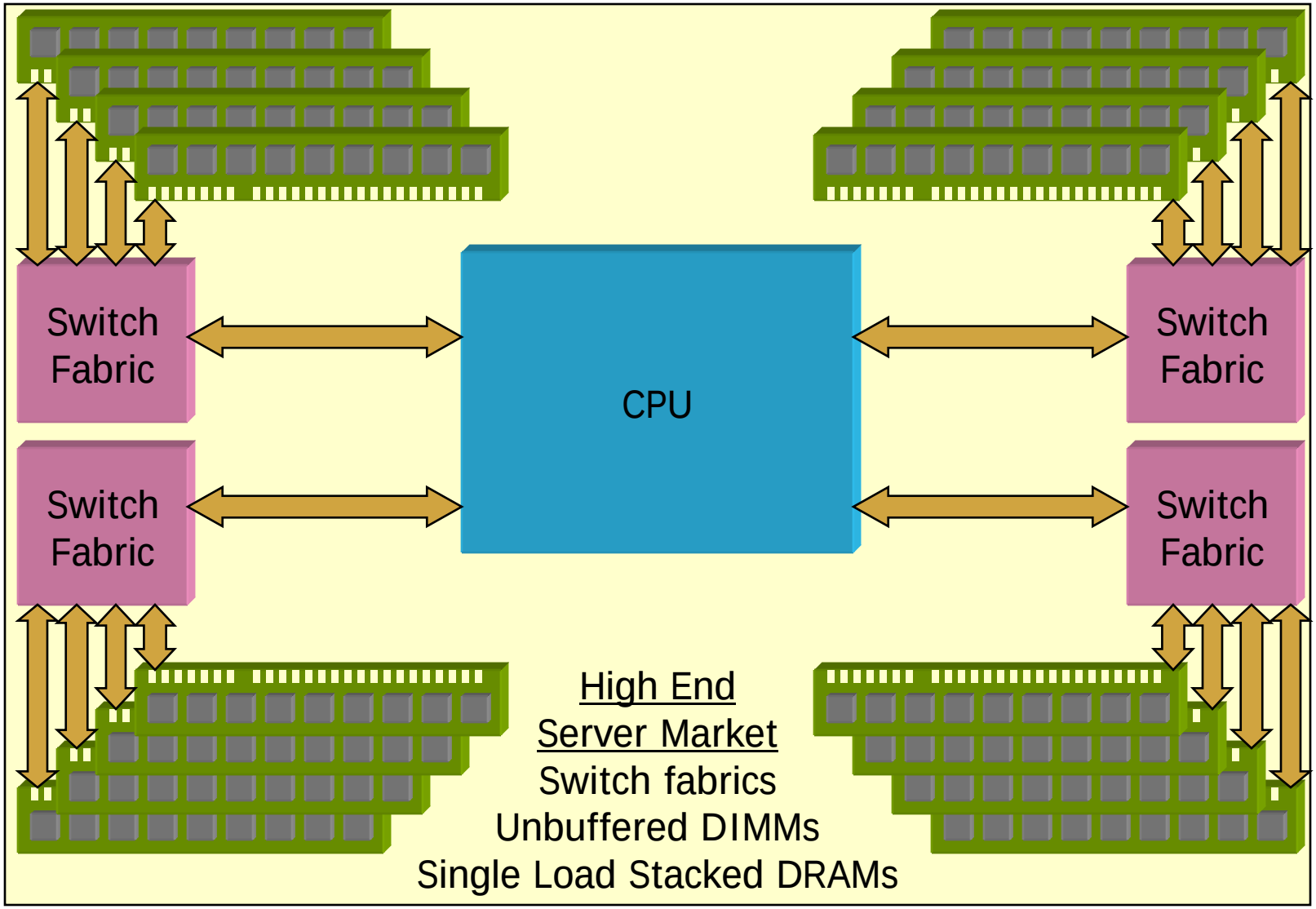


Notebook Market
Unbuffered SO-DIMM
Monolithic DRAMs



Workstation Market
Low End Server Market
Unbuffered DIMMs
Single Load Stacked DRAMs

Modules in DDR4 Generation



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Bill Gervasi

bilge@discobolusdesigns.com

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